

**NANOMAGNETIC AND
SPINTRONIC DEVICES
FOR ENERGY-EFFICIENT
MEMORY AND
COMPUTING**

In memory of my late great-uncle, N. Seshagiri, who inspired
my career in science and technology

Jayasimha Atulasimha

In memory of my uncle, Dalumama

Supriyo Bandyopadhyay

NANOMAGNETIC AND SPINTRONIC DEVICES FOR ENERGY-EFFICIENT MEMORY AND COMPUTING

Edited by

Jayasimha Atulasimha and Supriyo Bandyopadhyay

Virginia Commonwealth University, US

WILEY

This edition first published 2016 © 2016 John Wiley & Sons Ltd.

Registered office

John Wiley & Sons Ltd., The Atrium, Southern Gate, Chichester, West Sussex, PO19 8SQ, United Kingdom

For details of our global editorial offices, for customer services and for information about how to apply for permission to reuse the copyright material in this book please see our website at www.wiley.com.

The right of the author to be identified as the author of this work has been asserted in accordance with the Copyright, Designs and Patents Act 1988.

All rights reserved. No part of this publication may be reproduced, stored in a retrieval system, or transmitted, in any form or by any means, electronic, mechanical, photocopying, recording or otherwise, except as permitted by the UK Copyright, Designs and Patents Act 1988, without the prior permission of the publisher.

Wiley also publishes its books in a variety of electronic formats. Some content that appears in print may not be available in electronic books.

Designations used by companies to distinguish their products are often claimed as trademarks. All brand names and product names used in this book are trade names, service marks, trademarks or registered trademarks of their respective owners. The publisher is not associated with any product or vendor mentioned in this book.

Limit of Liability/Disclaimer of Warranty: While the publisher and author have used their best efforts in preparing this book, they make no representations or warranties with respect to the accuracy or completeness of the contents of this book and specifically disclaim any implied warranties of merchantability or fitness for a particular purpose. It is sold on the understanding that the publisher is not engaged in rendering professional services and neither the publisher nor the author shall be liable for damages arising herefrom. If professional advice or other expert assistance is required, the services of a competent professional should be sought.

The advice and strategies contained herein may not be suitable for every situation. In view of ongoing research, equipment modifications, changes in governmental regulations, and the constant flow of information relating to the use of experimental reagents, equipment, and devices, the reader is urged to review and evaluate the information provided in the package insert or instructions for each chemical, piece of equipment, reagent, or device for, among other things, any changes in the instructions or indication of usage and for added warnings and precautions. The fact that an organization or Website is referred to in this work as a citation and/or a potential source of further information does not mean that the author or the publisher endorses the information the organization or Website may provide or recommendations it may make. Further, readers should be aware that Internet Websites listed in this work may have changed or disappeared between when this work was written and when it is read. No warranty may be created or extended by any promotional statements for this work. Neither the publisher nor the author shall be liable for any damages arising herefrom.

Library of Congress Cataloging-in-Publication Data

Nanomagnetic and spintronic devices for energy-efficient memory and computing / edited by Jayasimha Atulasimha and Supriyo Bandyopadhyay.

pages cm

Includes bibliographical references and index.

ISBN 978-1-118-86926-0 (cloth)

1. Magnetic memory (Computers) 2. Spintronics. 3. Nanoelectronics. I. Atulasimha, Jayasimha, editor.

II. Bandyopadhyay, S., editor.

TK7895.M3N27 2016

621.39'73-dc23

2015033564

A catalogue record for this book is available from the British Library.

Cover image: The cover shows magnetic force micrographs of an array of 100-nm sized nanomagnets exhibiting single-domain behavior. Image courtesy of the Atulasimha group and Bandyopadhyay group.

Set in 10/12pt Times by Aptara Inc., New Delhi, India

Contents

About the Editors and Acknowledgments	xi
List of Contributors	xiii
Foreword	xvii
Preface	xix
1 Introduction to Spintronic and Nanomagnetic Computing Devices	1
<i>Jayasimha Atulasimha and Supriyo Bandyopadhyay</i>	
1.1 Spintronic Devices	1
1.2 Nanomagnetic Devices	3
1.2.1 <i>Use of Spin Torque to Switch Nanomagnets</i>	6
1.2.2 <i>Other Methodologies for Switching Nanomagnets</i>	6
1.3 Thinking beyond Traditional Boolean Logic	7
References	7
2 Potential Applications of all Electric Spin Valves Made of Asymmetrically Biased Quantum Point Contacts	9
<i>Nikhil Bhandari, Maitreya Dutta, James Charles, Junjun Wan, Marc Cahay, and S.T Herbert</i>	
2.1 Introduction	9
2.2 Quantum Point Contacts	11
2.3 Spin Orbit Coupling	14
2.3.1 <i>Rashba SOC (RSOC)</i>	15
2.3.2 <i>Dresselhaus SOC (DSOC)</i>	15
2.3.3 <i>Lateral Spin-Orbit Coupling (LSOC)</i>	16
2.4 Importance of Spin Relaxation in 1D Channels	18
2.5 Observation of a 0.5 Conductance Plateau in Asymmetrically Biased QPCs in the Presence of LSOC	20
2.5.1 <i>Early Experimental Results Using InAs QPCs</i>	20
2.5.2 <i>NEGF Conductance Calculations</i>	20
2.5.3 <i>Spin Texture Associated with Conductance Anomalies in QPCs</i>	23

2.5.4	<i>Prospect for Generation of Spin Polarized Current at Higher Temperature</i>	25
2.5.5	<i>Observation of Other Anomalous Conductance Plateaus in an Asymmetrically Biased InAs/In_{0.52}Al_{0.48} as QPCs</i>	26
2.6	Intrinsic Bistability near Conductance Anomalies	27
2.6.1	<i>Experimental Results</i>	28
2.6.2	<i>NEGF Simulations</i>	30
2.7	QPC Structures with Four In-plane SGs: Toward an All Electrical Spin Valve	43
2.7.1	<i>Preliminary Results on Four-gate QPCs</i>	43
2.7.2	<i>Experiments</i>	46
2.7.3	<i>Onset of Hysteresis and Negative Resistance Region</i>	50
2.8	Future Work	56
2.9	Summary	58
	Acknowledgments	60
	References	60
3	Spin-Transistor Technology for Spintronics/CMOS Hybrid Logic Circuits and Systems	65
	<i>Satoshi Sugahara, Yusuke Shuto, and Shuu'ichirou Yamamoto</i>	
3.1	Spin-Transistor and Pseudo-Spin-Transistor	65
3.1.1	<i>Spin – MOSFET</i>	66
3.1.2	<i>Pseudo-Spin-MOSFET</i>	69
3.2	Energy-Efficient Logic Applications of Spin-Transistors	72
3.2.1	<i>Power Gating with Nonvolatile Retention</i>	73
3.2.2	<i>Nonvolatile Bistable Circuits</i>	75
3.2.3	<i>Break-even Time</i>	76
3.3	Nonvolatile SRAM Technology	78
3.3.1	<i>Static Noise Margin of Nonvolatile SRAM</i>	79
3.3.2	<i>Energy Performance of NV-SRAM</i>	81
3.4	Application of Nonvolatile Bistable Circuits for Memory Systems	86
	References	88
4	Spin Transfer Torque: A Multiscale Picture	91
	<i>Yunkun Xie, Ivan Rungger, Kamaram Munira, Maria Stamenova, Stefano Sanvito, and Avik W. Ghosh</i>	
4.1	Introduction	91
4.1.1	<i>Background</i>	91
4.1.2	<i>STT Modeling: An Integrated Approach</i>	93
4.2	The Physics of Spin Transfer Torque	94
4.2.1	<i>Free-Electron Model for Magnetic Tunnel Junction</i>	96
4.3	First Principles Evaluation of TMR and STT	102
4.3.1	<i>The TMR Effect in the MgO Barrier</i>	104
4.3.2	<i>Currents and Torques in NEGF</i>	114
4.3.3	<i>First Principles Results on Spin Transfer Torque</i>	116
4.4	Magnetization Dynamics	119

4.4.1	<i>Landau-Lifshitz-Gilbert Equation</i>	119
4.4.2	<i>Spin Torque Switching in Presence of Thermal Fluctuations</i>	121
4.4.3	<i>Including Thermal Fluctuations: Stochastic LLG vs Fokker Planck</i>	122
4.5	Summary: Multiscaling from Atomic Structure to Error Rate	125
	Acknowledgments	129
	References	129
5	Magnetic Tunnel Junction Based Integrated Logics and Computational Circuits	133
	<i>Jian-Ping Wang, Mahdi Jamali, Angeline Klemm Smith, and Zhengyang Zhao</i>	
5.1	Introduction	133
5.2	GMR Based Field Programmable Devices	134
5.3	MTJ Based Field Programmable Devices	136
5.3.1	<i>MTJ Structure and TMR Ratio</i>	136
5.3.2	<i>MTJ Based Magneto-Logic</i>	137
5.3.3	<i>Utilization of STT in MTJ Based Magneto-Logic</i>	144
5.4	Information Transformation between Gates	145
5.4.1	<i>Direct Communication Using Charge Current</i>	146
5.4.2	<i>Magnetic Domain Walls for Information Transferring</i>	148
5.5	MTJ Based Logic-in-Memory Devices	148
5.6	Magnetic Quantum Cellular Automata	149
5.6.1	<i>Introduction and Background</i>	149
5.6.2	<i>Experimental Demonstrations</i>	150
5.7	All-Spin Based Magnetic Logic	155
5.7.1	<i>Nonlocal Lateral Spin Valve Background</i>	155
5.7.2	<i>Critical Parameters for Operation</i>	155
5.7.3	<i>Selected Review of Experimental Demonstrations</i>	156
5.7.4	<i>Applications to All-Spin Logic Devices</i>	158
5.8	Summary	161
	Acknowledgment	161
	References	162
6	Magnetization Switching and Domain Wall Motion Due to Spin Orbit Torque	165
	<i>Debanjan Bhowmik, OukJae Lee, Long You, and Sayeef Salahuddin</i>	
6.1	Introduction	165
6.2	Theory	166
6.2.1	<i>Rashba Effect</i>	168
6.2.2	<i>Spin Hall Effect</i>	169
6.3	Magnetic Switching Driven by Spin Orbit Torque	171
6.4	Domain Wall Motion Driven by Spin Orbit Torque	176
6.5	Applications of Spin Orbit Torque	184
6.6	Conclusion	186
	References	186

7	Magnonic Logic Devices	189
	<i>Alexander Khitun and Alexander Kozhanov</i>	
7.1	Introduction	189
7.2	Magnonic Logic Devices	197
7.3	Spin Wave-Based Logic Gates and Architectures	206
7.4	Discussion and Summary	212
	References	216
8	Strain Mediated Magnetoelectric Memory	221
	<i>N. Tiercelin, Y. Dusch, S. Giordano, A. Klimov, V. Preobrazhensky, and P. Pernod</i>	
8.1	Introduction	221
8.2	Concept of Unequivocal Strain- or Stress-Switched Nanomagnetic Memory	223
	8.2.1 <i>Magnetic Configuration and Equilibrium Positions</i>	223
	8.2.2 <i>Quasi-Static Stress-Mediated Switching</i>	225
8.3	LLG Simulations – Macrospin Model	226
	8.3.1 <i>Landau-Lifshitz-Gilbert Equation and Effective Magnetic Field</i>	226
	8.3.2 <i>Memory Parameters</i>	227
	8.3.3 <i>Results of the Macrospin Model</i>	228
8.4	LLG Simulations – Eshelby Approach	231
	8.4.1 <i>Geometry of the Memory Element</i>	232
	8.4.2 <i>Coupling with the External Magnetic Field</i>	233
	8.4.3 <i>Coupling with the External Electric Field and Elastic Stress</i>	234
	8.4.4 <i>Static Behavior of the System</i>	234
	8.4.5 <i>Dynamic Behavior of the System</i>	235
8.5	Stochastic Error Analysis	238
	8.5.1 <i>Statistical Mechanics of Magnetization in a Single-Domain Particle</i>	238
	8.5.2 <i>Switching Process within the Magnetoelectric Memory</i>	243
8.6	Preliminary Experimental Results	248
	8.6.1 <i>Piezoelectric Actuator with in-Plane Polarization</i>	248
	8.6.2 <i>Ferroelectric Relaxors with out-of-Plane Polarization</i>	249
	8.6.3 <i>Magnetoelastic Switching in a Magneto-Resistive Structure</i>	250
8.7	Conclusions	250
	Acknowledgments	252
	References	253
9	Hybrid Spintronics-Strainronics	259
	<i>Ayan K. Biswas, Noel D'Souza, Supriyo Bandyopadhyay, and Jayasimha Atulasimha</i>	
9.1	Introduction	259
	9.1.1 <i>Nanomagnetic Memory and Logic Devices: The Problem of Energy Dissipation in the Clocking Circuit</i>	260

9.1.2	<i>Switching Nanomagnets with Strain Could Drastically Reduce Energy Dissipation: Hybrid Spintronics-Straintronics Overview</i>	261
9.1.3	<i>Landau Lifshitz Gilbert (LLG) Equation</i>	263
9.2	Nanomagnetic Memory Switched with Strain	265
9.2.1	<i>Complete Magnetization Reversal (180° Switching): Complex out-of-Plane Dynamics</i>	265
9.2.2	<i>Switching the Magnetization between Two Mutually Perpendicular Stable Orientations and Extension to Stable Orientations with Angular Separation >90°</i>	268
9.2.3	<i>Complete 180° Switching with Stress Alone</i>	269
9.2.4	<i>Mixed Mode Switching of Magnetization by 180°: Acoustically Assisted Spin Transfer Torque (STT) Switching for Nonvolatile Memory</i>	273
9.3	Straintronic Clocking of Nanomagnetic Logic	276
9.3.1	<i>Two-State Dipole Coupled Nanomagnetic Logic</i>	276
9.3.2	<i>Four-state Multiferroic Nanomagnetic Logic (NML)</i>	279
9.3.3	<i>Switching Error in Dipole Coupled Nanomagnetic Logic (NML)</i>	283
9.3.4	<i>Straintronic Nanomagnetic Logic Devices (NML)</i>	284
9.4	Summary and Conclusions	286
	References	286
10	Unconventional Nanocomputing with Physical Wave Interference Functions	291
	<i>Santosh Khasanvis, Mostafizur Rahman, Prasad Shabadi, and Csaba Andras Moritz</i>	
10.1	Overview	291
10.2	Spin Waves Physical Layer for WIF Implementation	293
10.2.1	<i>Physical Fabric Components</i>	295
10.3	Elementary WIF Operators for Logic	298
10.4	Binary WIF Logic Design	303
10.4.1	<i>Binary WIF Full Adder</i>	303
10.4.2	<i>Parallel Counters</i>	306
10.4.3	<i>Benchmarking Binary WIF Circuits vs. CMOS</i>	309
10.4.4	<i>WIF Topology Exploration</i>	310
10.5	Multivalued WIF Logic Design	311
10.5.1	<i>Multivalued Operators and Implementation Using WIF</i>	312
10.5.2	<i>Multivalued Arithmetic Circuit Example: Quaternary Full Adder</i>	316
10.5.3	<i>Benchmarking of WIF Multivalued Circuits vs. Conventional CMOS</i>	318
10.5.4	<i>Input/Output Logic for Data Conversion between Binary and Radix-r Domains</i>	319
10.6	Microprocessors with WIF: Opportunities and Challenges	320
10.7	Summary and Future Work	326
	References	326
Index		329

About the Editors and Acknowledgments

Jayasimha Atulasimha

Jayasimha Atulasimha is Qimonda Associate Professor of Mechanical and Nuclear Engineering with a courtesy appointment in Electrical and Computer Engineering at the Virginia Commonwealth University, where he directs the Magnetism, Magnetic Materials and Magnetic Devices (M³) laboratory. He has authored or coauthored over 60 scientific articles including more than 40 journal publications on magnetostrictive materials, magnetization dynamics, and nanomagnetic computing and has given several invited talks at conferences, workshops and universities in the USA and abroad on these topics. His research interests include nanomagnetism, spintronics, magnetostrictive materials and nanomagnet-based computing devices. He received the NSF CAREER Award for 2013–2018. He currently serves on the Technical Committees for Spintronics, IEEE Nanotechnology Council, ASME Adaptive Structures and Material Systems, Device Research Conference (DRC), and as a Focus Topic organizer for the APS topical group on magnetism (GMAG). He is a member of ASME, APS and an IEEE Senior Member.

Supriyo Bandyopadhyay

Supriyo Bandyopadhyay is Commonwealth Professor in the Department of Electrical and Computer Engineering in Virginia Commonwealth University, Richmond, Virginia, USA, where he directs the Quantum Device Laboratory. His research interests are in broad areas of nanotechnology and focus on spintronics, nanomagnetism, energy-efficient and noncharge-based computing paradigms, optical properties of nanostructures, and self-assembly based nanosynthesis. He is the author/coauthor of over 300 peer reviewed research publications and has given over 100 invited or keynote talks in conferences, workshops and colloquia across four continents. He currently serves as the Chair of the Technical Committee on Spintronics within the Nanotechnology Council of the Institute of Electrical and Electronics Engineers (IEEE) and in the past served as the Chair of the Technical Committee on Compound Semiconductor Devices within the Electron Device Society of IEEE. He has served as an IEEE Distinguished Lecturer and also as a Vice President of the IEEE Nanotechnology Council. He is the winner of the Distinguished Scholarship Award at Virginia Commonwealth University, which is the highest award given by the university for scholarship to one faculty member each year, and

also won the faculty research award, the faculty interdisciplinary research award and the faculty service award from the College of Engineering at University of Nebraska where he was employed prior to coming to Virginia Commonwealth University. He currently serves on the editorial boards of six international journals and served on the editorial boards of seven other journals in the past. Dr Bandyopadhyay is a Fellow of the Institute of Electrical and Electronics Engineers, American Physical Society, Institute of Physics, the Electrochemical Society and the American Association for the Advancement of Science.

Acknowledgments

This work was supported by the US National Science Foundation under grants ECCS-1124714 and CCF-1216614. Jayasimha Atulasimha would also like to acknowledge the NSF CAREER grant CCF-1253370.

List of Contributors

Nikhil Bhandari

Spintronics and Vacuum Nanoelectronics Laboratory
University of Cincinnati
Cincinnati, OH, USA

Debanjan Bhowmik

Department of Electrical Engineering and Computer Sciences
University of California Berkeley
Berkeley, CA, USA

Ayan K. Biswas

Department of Electrical and Computer Engineering
Virginia Commonwealth University
Richmond, VA, USA

Marc Cahay

Spintronics and Vacuum Nanoelectronics Laboratory
University of Cincinnati
Cincinnati, OH, USA;
Physics Department
University of Cincinnati
Cincinnati, OH, USA

James Charles

School of Electrical Engineering
Purdue University
West Lafayette, IN, USA

Noel D'Souza

Department of Mechanical and Nuclear Engineering
Virginia Commonwealth University
Richmond, VA, USA

Y. Dusch

LIA LICS/LEMAL, IEMN UMR CNRS 8520, Univ. Lille, Centrale Lille
Lille, France

Maitreya Dutta

Spintronics and Vacuum Nanoelectronics Laboratory
University of Cincinnati
Cincinnati, OH, USA

Avik W. Ghosh

Charles L Brown School of Electrical and Computer Engineering
University of Virginia
Charlottesville, VA, USA

S. Giordano

LIA LICS/LEMAC, IEMN UMR CNRS 8520, Univ. Lille, Centrale Lille
Lille, France

S.T. Herbert

Department of Physics
Xavier University
Cincinnati, OH, USA

Mahdi Jamali

University of Minnesota
Minneapolis, MN, USA

Santosh Khasanvis

University of Massachusetts Amherst
Amherst, MA, USA

Alexander Khitun

University of California
Riverside, CA, USA

A. Klimov

International Associated Laboratory LIA LEMAC
Lille, France;
Moscow Institute of Radio Engineering and Automation MIREA
Moscow, Russia;
V.A. Kotelnikov Institute of Radioengineering and Electronics
Moscow, Russia

Alexander Kozhanov

Georgia State University
Atlanta, GA, USA

OukJae Lee

Department of Electrical Engineering and Computer Sciences
University of California Berkeley
Berkeley, CA, USA

Csaba Andras Moritz

University of Massachusetts Amherst
Amherst, MA, USA

Kamaram Munira

Center for Materials for Information Technology
University of Alabama
Tuscaloosa, AL, USA

P. Pernod

LIA LICS/LEMAC, IEMN UMR CNRS 8520, Univ. Lille, Centrale Lille
Lille, France

V. Preobrazhensky

LIA LICS/LEMAC, IEMN UMR CNRS 8520, Univ. Lille, Centrale Lille
Lille, France;
A.M. Prokhorov General Physics Institute RAS
Moscow, Russia

Mostafizur Rahman

University of Massachusetts Amherst
Amherst, MA, USA

Ivan Rungger

School of Physics, AMBER and CRANN Institute
Trinity College
Dublin, Ireland

Sayeef Salahuddin

Department of Electrical Engineering and Computer Sciences
University of California Berkeley
Berkeley, CA, USA

Stefano Sanvito

Center for Materials for Information Technology
University of Alabama
Tuscaloosa, AL, USA

Prasad Shabadi

University of Massachusetts Amherst
Amherst, MA, USA
Marvell Semiconductors

Yusuke Shuto

Imaging Science and Engineering Laboratory
Tokyo Institute of Technology
4259 Nagatsuta, Midori-ku, Yokohama, Japan

Angeline Klemm Smith

University of Minnesota,
Minneapolis, MN, USA

Maria Stamenova

School of Physics, AMBER and CRANN Institute
Trinity College
Dublin, Ireland

Satoshi Sugahara

Imaging Science and Engineering Laboratory
Tokyo Institute of Technology
4259 Nagatsuta, Midori-ku, Yokohama, Japan

N. Tiercelin

LIA LICS/LEMAL, IEMN UMR CNRS 8520, Univ. Lille, Centrale Lille
Lille, France

Junjun Wan

Intel Corporation
Hillsboro, OR, USA

Jian-Ping Wang

University of Minnesota
Minneapolis, MN, USA

Yunkun Xie

Charles L Brown School of Electrical and Computer Engineering
University of Virginia
Charlottesville, VA, USA

Shuu'ichirou Yamamoto

Imaging Science and Engineering Laboratory
Tokyo Institute of Technology
4259 Nagatsuta, Midori-ku, Yokohama, Japan

Long You

Department of Electrical Engineering and Computer Sciences
University of California Berkeley
Berkeley, CA, USA

Zhengyang Zhao

University of Minnesota
Minneapolis, MN, USA

Foreword

When I started out on my career, CMOS technology had just begun its domination in electronics. Although there are major challenges in continued scaling, no other technology was expected to be able to compete with CMOS commercially in the near future. However, the research community had always been interested in looking beyond CMOS and searching for alternative technologies. I was very fortunate to be surrounded by wise mentors and brilliant colleagues, who ultimately convinced me it would be fun to be in the arena of “beyond CMOS technologies.” On many occasions I wished somebody had written a book summarizing the most promising developments, saving professionals and students the time and aggravation of sifting through a plethora of many approaches. The fact that Jayasimha Atulasimha and Supriyo Bandyopadhyay are doing just that, putting together a collection of the latest and most promising developments in spintronics, is going to benefit not only young students and researchers new to the field, but will also provide a convenient reference for experts and experienced researchers to build their discoveries upon.

The field of spintronics has enjoyed rapid progress during the last decade, mostly due to the major challenge of excessive power dissipation in further CMOS scaling, which threatens perhaps a complete halt to scaling in the near future. As any active researcher in this field will tell you, the race to be the first to discover novel devices far beyond CMOS applications is both exhilarating as well as exhausting. It is therefore with great pleasure and honor that I am writing this foreword to introduce you to this timely treatise on the latest developments in this field, edited by recognized experts as well as my friends and colleagues, Supriyo Bandyopadhyay and Jayasimha Atulasimha.

This new book delivers a summary of the latest developments in spintronics in a way that is pleasantly digestible for any graduate level student and beyond, aspiring to excel in this field.

Professor Kang L. Wang
Distinguished Professor and Raytheon Chair in Electrical Engineering
University of California, Los Angeles

Preface

The complementary metal-oxide semiconductor (CMOS) device technology has dominated electronics for the last 70 years. CMOS has been able to scale down at an incredible pace, predicted by the famed Moore's law. However, it appears that further scaling of CMOS devices may encounter a road block by the end of the decade due to various issues, primarily among which is the rapid increase in heat dissipation as more and more devices are packed on to a chip with increasing densities.

There is also a strong need for computing devices that can operate with 2–3 orders of magnitude lower energy dissipation than current CMOS devices in embedded applications. Mobile and medical applications would prefer processors that would dissipate so little power that they can be run on energy harvested from the ambient without requiring a separate power source. If this comes to pass, it will open up myriad applications in wearable electronics, medical devices embedded to monitor the health of patients and sensor networks that monitor critical infrastructure such as buildings and bridges.

For these reasons, several new device concepts have been advanced as potential replacements for CMOS devices, or to complement CMOS devices for specific applications such as nonvolatile memory and logic, or to implement certain functionalities such as neuromorphic computing in a way better than CMOS devices can. They draw upon different physical mechanisms to elicit computational or signal processing activity. Among these different physical paradigms, spintronic and nanomagnetic devices form an important class both for the rich variety of physical phenomena on which these devices are based and the many different device concepts that they have spawned.

The editors hope that this book will provide the reader with a broad understanding of the key concepts behind spintronic and nanomagnetic devices as well as summarize the latest developments in this field. Questions and comments can be addressed to J. Atulasimha (jatulasimha@vcu.edu) and S. Bandyopadhyay (sbandy@vcu.edu).